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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,084	03/15/2004	Toshihiro Sawamoto	9319S-000662	9465

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EXAMINER	
SANDVIK, BENJAMIN P	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,084	SAWAMOTO, TOSHIHIRO	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on 7.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) 2 and 14 is/are withdrawn from consideration.

5)☒ Claim(s) 13 and 15 is/are allowed.

6)☒ Claim(s) 1, 3-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments regarding claims 1, 11, and 12 filed 7/27/2005 have been fully considered but they are not persuasive. On the grounds that the Lo reference fails to disclose or suggest projections, the examiner points out that solder balls 52 in Figure 2 are interpreted as projections to support the package. On the grounds that the Lo reference fails to disclose a third package that is independent from a second package, the examiner points out that the unitary substrate 10 is not considered as part of either the second or third package. The second package may comprise the chip 40 and its solder balls 52 and underfill 54 which is independent from the third package which may comprise the chip 42 and its solder balls 52 and underfill 54.

Applicant's arguments with respect to claims 4 and 6-10 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5, 11, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Lo et al (U.S. Patent 6507098).

With respect to **claim 1**, Lo teaches a first semiconductor package having a first semiconductor chip (Fig. 2, 26); a second semiconductor package supported on the first semiconductor package so that an end of the second semiconductor package is arranged directly above the first semiconductor chip (Fig. 2, 40); a third semiconductor package independent from said second semiconductor package, said third semiconductor package supported on the first semiconductor package so that an end of the third semiconductor package is arranged directly above the first semiconductor chip (Fig. 2, 42); a first projection supporting the end of the second semiconductor package directly above the first semiconductor chip (Fig. 2, center solder ball 52 on chip 40); and a second projection supporting the end of the third semiconductor package directly above the first semiconductor chip (Fig. 2, center solder ball 52 on chip 42).

With respect to **claim 3**, Lo teaches a second semiconductor package that is spaced apart from a third semiconductor package (Fig. 2, 40 and 42).

With respect to **claim 5**, Lo teaches that a space between the first semiconductor package and the second semiconductor package is filled with resin (Fig. 2, 36).

With respect to **claim 11**, Lo teaches a first package having an electronic component (Fig. 2, 26); a second package supported on the first package so that

an end of the second package is arranged directly above the electronic component (Fig. 2, 40); and a third package that is independent from the second package, said third package is supported on the first package so that an end of the third package is arranged directly above the electronic component (Fig. 2, 42); a first projection supporting the end of the second package directly above the electronic component (Fig. 2, center solder ball 52 on chip 40); and a second projection supporting the end of the third package directly above the electronic component (Fig. 2, center solder ball 52 on chip 42).

With respect to **claim 12**, Lo teaches a first semiconductor package having a semiconductor chip (Fig. 2, 10); a second semiconductor package supported on the first semiconductor package so that an end of the second semiconductor package is arranged directly above the semiconductor chip (Fig. 2, 40); a third semiconductor package that is independent of said second semiconductor package, said third semiconductor package is supported on the first semiconductor package so that an end of the third semiconductor package is arranged directly above the semiconductor chip (Fig. 2, 42); a first projection supporting the end of the second semiconductor package directly above the semiconductor chip (Fig. 2, center solder ball 52 on chip 40); a second projection supporting the end of the third semiconductor package directly above the semiconductor chip (Fig. 2, center solder ball 52 on chip 42); and a motherboard having the second semiconductor package and the third semiconductor package (Fig. 2, 100).

Claims 4, 6-8 rejected under 35 U.S.C. 103(a) as being unpatentable over Lo, in view of Degani et al (U.S. Patent #6369444).

With respect to **claim 4**, Lo teaches all of the limitations of claim 1, but does not teach that the second and third semiconductor packages are different in at least one of size, thickness, and material. Degani teaches that a second semiconductor package (Fig. 1, 12 and 13) is a different size than a third semiconductor package (Fig. 1, 11, and 13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the second and third semiconductor packages different sizes as taught by Degani in order to accommodate for spatial constraints in the package.

With respect to **claims 6-8**, Lo teaches all of the limitations of claim 1, and also teaches that the first semiconductor package has a first carrier substrate (Fig. 2, 100), a second carrier substrate (Fig. 2, 10), a bump that is bonded to the first carrier substrate and that holds the second carrier substrate on or above the first semiconductor chip (Fig. 2, 48), a seal for sealing the second semiconductor chips (Fig. 2, 46), that the bump is arranged on the second carrier substrate away from the mounting region of the first semiconductor chip (Fig. 2, 48), and that the projection is arranged so that the second carrier substrate is supported at four corners. Lo does not teach the first semiconductor chip being flip chip mounted on or above the first carrier substrate, or that the second semiconductor package has plural semiconductor chips mounted by a ball grid array or chip size

package on or above a second carrier substrate. Degani teaches that the first semiconductor chip (Fig. 1, 15) is flip chip mounted on the first carrier substrate (Fig. 1, 24) and that there is a plurality of second semiconductor chips (Fig. 1, 12 and 13) mounted on a second carrier substrate (Fig. 1, 12 and 14) by flip chip methods. It would have been obvious to one of ordinary skill in the art at the time the invention was made to flip-chip mount the first semiconductor chip onto the first carrier substrate in order to decrease the size of the package, and to provide multiple semiconductor chips that are flip-chip mounted on the second carrier substrate in order to increase the number of functions that can be performed on the package.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo and Degani, further in view of Senba et al (U.S. Patent #5973392).

With respect to **claim 9**, Lo and Degani teach all of the limitations of claim 6, but do not teach that the first semiconductor chip comprises a logical operation element and the second semiconductor chips comprises memory elements. Senba teaches a first semiconductor chip that comprises a logical operation element (Fig. 8b, 3) and second semiconductor chips comprise memory elements (Fig. 8b, 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to select the first chip to comprise a logical operator and the second chips to comprise memory elements as taught by Senba in order to make a three dimensional memory device.

With respect to **claim 10**, Lo and Degani teach all of the limitations of claim 6, but do not teach that the second semiconductor chips have a three-dimensionally mounted structure. Senba teaches a three dimensionally mounted structure (Fig. 8b). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the package of Lo and Degani a three dimensionally mounted structure in order to increase the functional capabilities on the package.

Allowable Subject Matter

Claims 13 and 15 allowed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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